CLAIM AMENDMENTS

1. (currently amended) A TTCM (Turbo Trellis Coded Modulation) encoder that encodes a plurality of input bits according to a rate control sequence, the encoder comprising:

a top interleaver operably coupled selectively to interleave at least some input bits of the plurality of input bits;

a top rate 2/4 constituent trellis encoder, communicatively coupled to the top interleaver and operable to receive selectively interleaved bits there from, that is operable to encode the selectively interleaved bits that have been interleaved by the top interleaver;

a bottom interleaver operably coupled selectively to interleave at least some input bits of the plurality of input bits;

a bottom rate 2/4 constituent trellis encoder, communicatively coupled to the bottom interleaver and operable to receive selectively interleaved bits there from, that is operable to encode the selectively interleaved bits that have been interleaved by the bottom interleaver;

a MUX (Multiplexor) that alternatively selects encoded bits that are output from the top rate 2/4 constituent trellis encoder and the bottom rate 2/4 constituent trellis encoder to produce a first plurality of multiplexed bits and a second plurality of multiplexed bits;

a puncturing functional block that is operable selectively to puncture the first plurality of multiplexed bits output from the MUX according to a first RC (Rate Control) of the rate control sequence to produce a first encoded symbol;

wherein the puncturing functional block is operable selectively to puncture the second plurality of multiplexed bits output from the MUX according to a second RC of the rate control sequence to produce a second encoded symbol;

a symbol mapper that maps the first encoded symbol according to the first RC thereby generating a first mapped symbol;

wherein the symbol mapper maps the second encoded symbol according to the second RC thereby generating a second mapped symbol;

wherein the first RC of the rate control sequence corresponds to a first modulation that includes a first mapping of either a first 16 QAM (Quadrature Amplitude Modulation) constellation or a first 16 APSK (16 Asymmetric Phase Shift Keying) constellation;

wherein the second RC of the rate control sequence corresponds to a second modulation that includes a second mapping of either a second 16 QAM constellation or a second 16 APSK constellation;

wherein the first mapped symbol and the second mapped symbol form an encoded signal; and

wherein the encoded signal has a bandwidth efficiency that is greater than approximately 3 bit/s/Hz (bits per second per Hertz).

2. (original) The encoder of claim 1, further comprising:

a rate control sequencer that provides the first RC and the second RC of the rate control sequence to the puncturing functional block and to the symbol mapper.

3. (original) The encoder of claim 1, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation.

4. (original) The encoder of claim 1, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation.

5. (original) The encoder of claim 1, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, the second RC, and a fourth RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation;

the third RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation; and

the fourth RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation.

6. (original) The encoder of claim 1, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation.

7. (original) The encoder of claim 1, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation.

8. (original) The encoder of claim 1, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation;

the third RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation; and

the fourth RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation.

9. (original) The encoder of claim 1, wherein:

the first encoded symbol includes 1 uncoded bit; and

the second encoded symbol includes 2 uncoded bits.

10. (original) The encoder of claim 1, wherein:

the top interleaver operably coupled selectively to interleave at least some input bits of the plurality of input bits interleaves only odd positioned bits of the plurality of input bits; and

the bottom interleaver operably coupled selectively to interleave at least some input bits of the plurality of input bits interleaves only even positioned bits of the plurality of input bits.

11. (original) The encoder of claim 1, wherein:

the first plurality of multiplexed bits output from the MUX according to the first RC of the rate control sequence includes 4 multiplexed bits;

the puncturing functional block selectively punctures 1 bit of the 4 multiplexed bits; and

the puncturing functional block employs the 3 non-punctured bits of the 4 multiplexed bits and 1 uncoded bit to produce the first encoded symbol.

12. (original) The encoder of claim 1, wherein:

the second plurality of multiplexed bits output from the MUX according to the second RC of the rate control sequence includes 4 multiplexed bits;

the puncturing functional block selectively punctures 2 bits of the 4 multiplexed bits; and

the puncturing functional block employs the 2 non-punctured bits of the 4 multiplexed bits and 2 uncoded bits to produce the second encoded symbol.

13. (original) The encoder of claim 1, wherein:

the top rate 2/4 constituent trellis encoder is implemented using 2 separate rate 2/4 constituent trellis encoders;

the first plurality of multiplexed bits output from the MUX according to the first RC of the rate control sequence includes 8 multiplexed bits;

the puncturing functional block selectively punctures 4 bits of the 8 multiplexed bits; and

the puncturing functional block employs the 4 non-punctured bits of the 8 multiplexed bits to produce the first encoded symbol.

14. (original) The encoder of claim 1, wherein:

the bottom rate 2/4 constituent trellis encoder is implemented using 2 separate rate 2/4 constituent trellis encoders;

the second plurality of multiplexed bits output from the MUX according to the second RC of the rate control sequence includes 8 multiplexed bits;

the puncturing functional block selectively punctures 4 bits of the 8 multiplexed bits; and

the puncturing functional block employs the 4 non-punctured bits of the 8 multiplexed bits to produce the second encoded symbol.

15. (original) The encoder of claim 1, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, and a fiber-optic communication system.

16. (currently amended) A TTCM (Turbo Trellis Coded Modulation) encoding method that encodes a plurality of input bits according to a rate control sequence, the method comprising:

selectively interleaving at least some input bits of the plurality of input bits to generate a first plurality of selectively interleaved bits;

encoding the first plurality of selectively interleaved bits;

selectively interleaving at least some input bits of the plurality of input bits to generate a second plurality of selectively interleaved bits;

encoding the second plurality of selectively interleaved bits;

alternatively selecting encoded bits from the encoded first plurality of selectively interleaved bits and the encoded second plurality of selectively interleaved bits to produce a first plurality of multiplexed bits and a second plurality of multiplexed bits, respectively;

selectively puncturing the first plurality of multiplexed bits according to a first RC (Rate Control) of the rate control sequence to produce a first encoded symbol,

wherein the first RC of the rate control sequence corresponds to a first modulation that includes a first mapping of either a first 16 QAM (Quadrature Amplitude Modulation) constellation or a first 16 APSK (16 Asymmetric Phase Shift Keying) constellation;

selectively puncturing the second plurality of multiplexed bits according to a second RC of the rate control sequence to produce a second encoded symbol, wherein the second RC of the rate control sequence corresponds to a second modulation that includes a second mapping of either a second 16 QAM constellation or a second 16 APSK constellation;

symbol mapping the first encoded symbol according to the first RC thereby generating a first mapped symbol;

symbol mapping the second encoded symbol according to the second RC thereby generating a second mapped symbol; and

forming an encoded signal using the first mapped symbol and the second mapped symbol, wherein the encoded signal has a bandwidth efficiency that is greater than approximately 3 bit/s/Hz (bits per second per Hertz).

17. (original) The method of claim 16, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation.

18. (original) The method of claim 16, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation.

19. (original) The method of claim 16, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, the second RC, and a fourth RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation;

the third RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation; and

the fourth RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation.

20. (original) The method of claim 16, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation.

21. (original) The method of claim 16, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation.

22. (original) The method of claim 16, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation;

the third RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation; and

the fourth RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation.

23. (original) The method of claim 16, wherein:

the first encoded symbol includes 1 uncoded bit; and

the second encoded symbol includes 2 uncoded bits.

24. (original) The method of claim 16, wherein:

the selectively interleaving of at least some input bits of the plurality of input bits includes interleaving only odd positioned bits of the plurality of input bits; and

the selectively interleaving of at least some input bits of the plurality of input bits includes interleaving only even positioned bits of the plurality of input bits.

25. (original) The method of claim 16, wherein:

the first plurality of multiplexed bits according to the first RC of the rate control sequence includes 4 multiplexed bits;

the selectively puncturing includes puncturing 1 bit of the 4 multiplexed bits; and

employing the 3 non-punctured bits of the 4 multiplexed bits and 1 uncoded bit to produce the first encoded symbol.

26. (original) The method of claim 16, wherein:

the second plurality of multiplexed bits according to the second RC of the rate control sequence includes 4 multiplexed bits;

the selectively puncturing includes puncturing 2 bits of the 4 multiplexed bits; and

employing the 2 non-punctured bits of the 4 multiplexed bits and 2 uncoded bits to produce the second encoded symbol.

27. (original) The method of claim 16, wherein:

the first plurality of multiplexed bits according to the first RC of the rate control sequence includes 8 multiplexed bits;

the selectively puncturing includes puncturing 4 bits of the 8 multiplexed bits; and

employing the 4 non-punctured bits of the 8 multiplexed bits to produce the first encoded symbol.

28. (original) The method of claim 16, wherein:

the second plurality of multiplexed bits according to the second RC of the rate control sequence includes 8 multiplexed bits;

the selectively puncturing includes puncturing 4 bits of the 8 multiplexed bits; and

employing the 4 non-punctured bits of the 8 multiplexed bits to produce the second encoded symbol.

29. (original) The method of claim 16, wherein:

the method is performed within an encoder that is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, and a fiber-optic communication system.

30. (currently amended) A TTCM (Turbo Trellis Coded Modulation) encoder that encodes a plurality of input bits according to a rate control sequence, the encoder comprising:

at least one constituent trellis encoder that is operable to encode the plurality of input bits thereby generating a first plurality of encoded bits and a second plurality of encoded bits;

a puncturing functional block that is operable selectively to puncture the first plurality of encoded bits according to a first RC (Rate Control) of the rate control sequence to produce a first encoded symbol;

wherein the puncturing functional block is operable selectively to puncture the second plurality of encoded bits according to a second RC of the rate control sequence to produce a second encoded symbol;

a symbol mapper that maps the first encoded symbol according to the first RC thereby generating a first mapped symbol;

wherein the symbol mapper maps the second encoded symbol according to the second RC thereby generating a second mapped symbol;

wherein the first RC of the rate control sequence corresponds to a first modulation that includes a first mapping of either a first 16 QAM (Quadrature Amplitude Modulation) constellation or a first 16 APSK (16 Asymmetric Phase Shift Keying) constellation;

wherein the second RC of the rate control sequence corresponds to a second modulation that includes a second mapping of either a second 16 QAM constellation or a second 16 APSK constellation;

wherein the first mapped symbol and the second mapped symbol form an encoded signal; and

wherein the encoded signal has a bandwidth efficiency that is greater than approximately 3 bit/s/Hz (bits per second per Hertz).

31. (original) The encoder of claim 30, further comprising:

a rate control sequencer that provides the first RC and the second RC of the rate control sequence to the puncturing functional block and to the symbol mapper.

32. (original) The encoder of claim 30, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation.

33. (original) The encoder of claim 30, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation.

34. (original) The encoder of claim 30, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, the second RC, and a fourth RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation;

the third RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation; and

the fourth RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation.

35. (original) The encoder of claim 30, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation.

36. (original) The encoder of claim 30, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the plurality of RCs arranged in the period includes the first RC, a third RC, and the second RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation.

37. (original) The encoder of claim 30, wherein:

the rate control sequence includes a plurality of RCs arranged in a period;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation;

the third RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation; and

the fourth RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation.

38. (original) The encoder of claim 30, wherein:

the first encoded symbol includes 1 uncoded bit; and

the second encoded symbol includes 2 uncoded bits.

39. (original) The encoder of claim 30, wherein:

the at least one constituent trellis encoder is a top rate 2/4 constituent trellis encoder;

the first plurality of encoded bits according to the first RC of the rate control sequence includes 4 encoded bits;

the puncturing functional block selectively punctures 1 bit of the 4 encoded bits; and

the puncturing functional block employs the 3 non-punctured bits of the 4 encoded bits and 1 uncoded bit to produce the first encoded symbol.

40. (original) The encoder of claim 30, wherein:

the at least one constituent trellis encoder is a bottom rate 2/4 constituent trellis encoder;

the second plurality of encoded bits according to the second RC of the rate control sequence includes 4 encoded bits;

the puncturing functional block selectively punctures 2 bits of the 4 encoded bits; and

the puncturing functional block employs the 2 non-punctured bits of the 4 encoded bits and 2 uncoded bits to produce the second encoded symbol.

41. (original) The encoder of claim 30, wherein:

the at least one constituent trellis encoder is a top rate 2/4 constituent trellis encoder that is implemented using 2 separate rate 2/4 constituent trellis encoders;

the first plurality of encoded bits according to the first RC of the rate control sequence includes 8 encoded bits;

the puncturing functional block selectively punctures 4 bits of the 8 encoded bits; and

the puncturing functional block employs the 4 non-punctured bits of the 8 encoded bits to produce the first encoded symbol.

42. (original) The encoder of claim 30, wherein:

the at least one constituent trellis encoder is a bottom rate 2/4 constituent trellis encoder that is implemented using 2 separate rate 2/4 constituent trellis encoders;

the second plurality of encoded bits according to the second RC of the rate control sequence includes 8 encoded bits;

the puncturing functional block selectively punctures 4 bits of the 8 encoded bits; and

the puncturing functional block employs the 4 non-punctured bits of the 8 encoded bits to produce the second encoded symbol.

43. (original) The encoder of claim 30, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, and a fiber-optic communication system.

44. (currently amended) A TTCM (Turbo Trellis Coded Modulation) encoder that encodes a plurality of input bits according to a rate control sequence, the encoder comprising:

at least one constituent trellis encoder that is operable to encode the plurality of input bits thereby generating a first plurality of encoded bits, a second plurality of encoded bits, and a third plurality of encoded bits;

a puncturing functional block that is operable selectively to puncture the first plurality of encoded bits according to a first RC (Rate Control) of the rate control sequence to produce a first encoded symbol;

wherein the puncturing functional block is operable selectively to puncture the second plurality of encoded bits according to a second RC of the rate control sequence to produce a second encoded symbol;

wherein the puncturing functional block is operable selectively to puncture the third plurality of encoded bits according to a third RC of the rate control sequence to produce a third encoded symbol;

a symbol mapper that maps the first encoded symbol according to the first RC thereby generating a first mapped symbol;

wherein the symbol mapper maps the second encoded symbol according to the second RC thereby generating a second mapped symbol;

wherein the symbol mapper maps the third encoded symbol according to the third RC thereby generating a third mapped symbol;

wherein the first RC of the rate control sequence corresponds to a first modulation that includes a first mapping of either a first 16 QAM (Quadrature

Amplitude Modulation) constellation or a first 16 APSK (16 Asymmetric Phase Shift Keying) constellation;

wherein the second RC of the rate control sequence corresponds to a second modulation that includes a second mapping of either a second 16 QAM constellation or a second 16 APSK constellation;

wherein the third RC of the rate control sequence corresponds to a third modulation that includes a first mapping of a first QPSK (Quadrature Phase Shift Key) constellation;

wherein the first mapped symbol, the second mapped symbol, and the third mapped symbol form an encoded signal; and

wherein the encoded signal has a bandwidth efficiency that is greater than approximately 3 bit/s/Hz (bits per second per Hertz).

45. (original) The encoder of claim 44, further comprising:

a rate control sequencer that provides the first RC and the second RC of the rate control sequence to the puncturing functional block and to the symbol mapper.

46. (original) The encoder of claim 44, wherein:

the rate control sequence includes 9 RCs arranged in a period;

the 9 RCs arranged in the period include the first RC, 7 occurrences of the second RC, and the third RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to the third modulation that includes the first mapping of the first QPSK constellation.

47. (original) The encoder of claim 44, wherein:

the rate control sequence includes 9 RCs arranged in a period;

the 9 RCs arranged in the period include the first RC, 3 occurrences of the second RC, an additional occurrence of the first RC, 3 additional occurrences of the second RC, and the third RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to the third modulation that includes the first mapping of the first QPSK constellation.

48. (original) The encoder of claim 44, wherein:

the rate control sequence includes 9 RCs arranged in a period;

the 9 RCs arranged in the period include 2 occurrences of the first RC, 2 occurrences of the second RC, 2 additional occurrences of the first RC, 2 additional occurrences of the second RC, and the third RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 QAM constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 QAM constellation; and

the third RC corresponds to the third modulation that includes the first mapping of the first QPSK constellation.

49. (original) The encoder of claim 44, wherein:

the rate control sequence includes 9 RCs arranged in a period;

the 9 RCs arranged in the period include the first RC, 7 occurrences of the second RC, and the third RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to the third modulation that includes the first mapping of the first QPSK constellation.

50. (original) The encoder of claim 44, wherein:

the rate control sequence includes 9 RCs arranged in a period;

the 9 RCs arranged in the period include the first RC, 3 occurrences of the second RC, an additional occurrence of the first RC, 3 additional occurrences of the second RC, and the third RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to the third modulation that includes the first mapping of the first QPSK constellation.

51. (original) The encoder of claim 44, wherein:

the rate control sequence includes 9 RCs arranged in a period;

the 9 RCs arranged in the period include 2 occurrences of the first RC, 2 occurrences of the second RC, 2 additional occurrences of the first RC, 2 additional occurrences of the second RC, and the third RC;

the first RC corresponds to the first modulation that includes the first mapping of the first 16 APSK constellation;

the second RC corresponds to the second modulation that includes the second mapping of the second 16 APSK constellation; and

the third RC corresponds to the third modulation that includes the first mapping of the first QPSK constellation.

52. (original) The encoder of claim 44, wherein:

the first encoded symbol includes 1 uncoded bit; and

the second encoded symbol includes 2 uncoded bits.

53. (original) The encoder of claim 44, wherein:

the at least one constituent trellis encoder is a top rate 2/4 constituent trellis encoder;

the first plurality of encoded bits according to the first RC of the rate control sequence includes 4 encoded bits;

the puncturing functional block selectively punctures 1 bit of the 4 encoded bits; and

the puncturing functional block employs the 3 non-punctured bits of the 4 encoded bits and 1 uncoded bit to produce the first encoded symbol.

54. (original) The encoder of claim 44, wherein:

the at least one constituent trellis encoder is a bottom rate 2/4 constituent trellis encoder;

the second plurality of encoded bits according to the second RC of the rate control sequence includes 4 encoded bits;

the puncturing functional block selectively punctures 2 bits of the 4 encoded bits; and

the puncturing functional block employs the 2 non-punctured bits of the 4 encoded bits and 2 uncoded bits to produce the second encoded symbol.

55. (original) The encoder of claim 44, wherein:

the at least one constituent trellis encoder is a top rate 2/4 constituent trellis encoder that is implemented using 2 separate rate 2/4 constituent trellis encoders;

the first plurality of encoded bits according to the first RC of the rate control sequence includes 8 encoded bits;

the puncturing functional block selectively punctures 4 bits of the 8 encoded bits; and

the puncturing functional block employs the 4 non-punctured bits of the 8 encoded bits to produce the first encoded symbol.

56. (original) The encoder of claim 44, wherein:

the at least one constituent trellis encoder is a bottom rate 2/4 constituent trellis encoder that is implemented using 2 separate rate 2/4 constituent trellis encoders;

the second plurality of encoded bits according to the second RC of the rate control sequence includes 8 encoded bits;

the puncturing functional block selectively punctures 4 bits of the 8 encoded bits; and

the puncturing functional block employs the 4 non-punctured bits of the 8 encoded bits to produce the second encoded symbol.

57. (original) The encoder of claim 44, wherein:

the encoder is implemented within a communication device; and

the communication device is implemented within at least one of a satellite communication system, an HDTV (High Definition Television) communication system, a cellular communication system, a microwave communication system, a point-to-point communication system, a uni-directional communication system, a bi-directional communication system, a one to many communication system, and a fiber-optic communication system.